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PHYSICS AND TECHNOLOGY OF POWER MOSFETs

A DISSERTATION

SUBMITTED TO THE DEPARTMENT OF ELECTRICAL ENGINEERING

AND THE COMMITTEE ON GRADUATE STUDIES

OF STANFORD UNIVERSITY

IN PARTIAL FULFILLMENT OF THE REQUIREMENTS

FOR THE DEGREE OF

DOCTOR OF PHILOSOPHY

By

Shi-Chung Sun

February 1982

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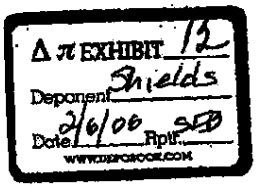
Sun, Shi-Chang

PHYSICS AND TECHNOLOGY OF POWER MOSFETS

Stanford University PH.D. 1982



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I certify that I have read this thesis and that in my opinion it is fully adequate, in scope and quality, as a dissertation for the degree of Doctor of Philosophy.

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ABSTRACT

The power-handling capability of power MOSFETs is beginning to rival bipolar transistors. This new capability is based on the use of double-diffusion techniques to achieve short active channels and on the incorporation of a lightly doped drift region between the channel and drain contact, which largely supports the applied voltage. In this work, quantitative models for on-resistance are developed for the three most commonly used structures--the LDMOS, VDMOS, and VMOS. These models are useful in optimizing a particular device and in comparing all of them for a specific application.

Small surface spacings and geometries in the VDMOS result in two-region saturation I-V characteristics that can be explained in terms of the depletion of the epitaxial region between channel junctions. A first-order I-V solution demonstrates the dependence of this phenomenon on the physical structure. The degradation of this effect on device transconductance can be more severe than thermal effects in high-current operation.

Breakdown limitations and parasitic bipolar latchback are examined in detail and are related to device structure and processing. The switching requirement dV/dt during turn-off places a severe constraint on channel thickness and doping concentrations under most layout conditions. The punchthrough limit dominates only when the channel contacts are adjacent to the edges of the gates. The differences in performance and on-resistance between power-MOS and bipolar devices are studied in terms of carrier injection and transport mechanisms.

Knowledge of electron mobility in both inversion and accumulation layers is essential for accurate modeling of power MOSFETs. This need resulted in an extensive set of mobility measurements as a function of various processing parameters. Analytical expressions are derived to predict mobility over a wide range of conditions, and the results will have significant impact when optimizing the performance of all types of MOS structures.

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TABLES

SYMBOLS

a	upper width of the trapezoid impurity gradient of the emitter-base junction
A	chip area effective channel-drain junction area
A_{cell}	cell area
b_1	length of the trapezoid
BV	avalanche breakdown voltage
BV_{CBO}	open emitter collector to base breakdown voltage
BV_{CEO}	open base collector to emitter breakdown voltage
BV_{cy}	avalanche breakdown voltage of the $N^+N^-P^-$ diode
BV_{DSS}	drain-to-source breakdown voltage
BV_{PP}	plane-junction breakdown voltage with a cylindrical N^+ junction
BV_{PT}	avalanche breakdown voltage of the $N^+N^-P^-$ diode with parallel-plane abrupt junctions
C*	constant = 0.8
C_{BC}	base-collector capacitance
C_E	emitter-base capacitance
C_{GS}	gate-to-source capacitance
C_{in}	input capacitance
C_{NE}	neutral capacitance
C_o	gate-oxide capacitance per unit area
C_{TE}	emitter-base transition capacitance
d_{eff}	effective channel length under the source
d_{epi}	epitaxial-layer thickness
dn	width of the N^- region of the $N^+N^-P^-$ diode
D_n	electron diffusivity

E	electric field
E_g	energy band gap
E_{crit}	critical field of semiconductor avalanche breakdown
E_{ox}	electric field in the oxide
E_s	electric field at the semiconductor surface
E_{eff}	effective field in the inversion layer
f_T	common-emitter cutoff frequency
g_d	dc drain conductance of the MOSFET
g_m	small-signal transconductance of the MOSFET
$g_{m(max)}$	maximum value of transconductance
G	Gummel number
h	height of the trapezoid
i_x	transverse current
I	current in the trapezoid
I_B	base current
I_{CBO}	collector-to-base reverse leakage current
I_{CEO}	collector-to-emitter leakage current
I_D, I_{DS}	drain current of the MOSFET
I_{DJ}	drain current of the JFET
I_{DSAT}	drain current at saturation of the MOSFET
I_E	emitter current
I_{accum}	accumulation current
J	current density
J_D	switching current density
k	Boltzmann's constant
l_c	collector-region thickness of the bipolar transistor

L	exponential length constant spacing of the V-groove mask length of the element
L'	effective length of the N^- region of the lateral DMOS
L_B	bulk Debye length
L_{eff}	channel length of enhancement-mode MOSFET
L'_{eff}	channel length of depletion-mode MOSFET
L_T	spacing between channel junctions at semiconductor surface
M	low-level multiplication factor
n_D	constant = 4
n_i	intrinsic carrier concentration
N_A	acceptor impurity concentration
N_D	donor impurity concentration
N_{inv}	induced carrier in the inversion layer per unit area
N_{it}	interface state per unit area
$N_{A(sub)}$	substrate doping concentration
$N_B, N_{D(epi)}$	epitaxial-layer doping concentration
N_{cell}	number of cells for a given chip area
N_T	number of trapezoids
N_c	channel doping concentration
N_{max}	maximum channel doping concentration
N_{peak}	maximum surface impurity concentration in the channel
N_{eff}	effective doping concentration
$p(o)$	injected hole concentration at base-collector junction
q	electric charge
Q_B	depletion charge per unit area total channel impurity density (per unit area)
Q_f	fixed-oxide charge per unit area at oxide/semiconductor interface

Q_s	total induced charge per unit area in the semiconductor
Q_D	depletion-layer charge on the drain side
r_o	radius of a circle
r_1	effective radius of the current source at the end of the channel
r_2	effective radius of the current sink at the N^+ contact
r_c	collector resistance
r_E	emitter resistance
r_j	channel junction depth
r_{jn}	N^+ drain diffusion depth
R_O	channel sheet resistance
R_q	epitaxial-layer bulk resistance
R_D	depletion-mode channel resistance
R_E	enhancement-mode channel resistance
R_{JFET}	JFET channel resistance
R_P	pinched channel resistance
R_s	sheet resistance
t_{ox}	oxide thickness
T	temperature (°K)
$\bar{U}$	normalized potential drop
v*	constant = 2.4×10^7 cm/sec
v_{SAT}	scattering-limited velocity
V(x)	voltage across region ③ in the VMOS
V_{BE}	base-emitter voltage of the bipolar transistor
V_D, V_{DS}	drain-source voltage of the MOSFET
V_{DSAT}	drain saturation voltage
V_{FB}	flatband voltage

V_{GS}	gate-source voltage
V_{oc}	crossover voltage between ohmic and space-charge-limited currents
V_C	voltage drop across the epitaxial layer
V_{SJ}	source voltage of the JFET
V_{DJ}	drain voltage of the JFET
V_T	threshold voltage
V_{TE}	threshold voltage of the enhancement-mode MOSFET
V_{TD}	threshold voltage of the depletion-mode MOSFET
V_a	applied potential
V_p	punchthrough voltage of the $N^+N^-P^-$ diode pinchoff voltage of the JFET
V_{PT}	drain-to-source punchthrough voltage
V_{ox}	voltage drop across the oxide
V_G	gate-to-ground voltage
V_{BS}	substrate bias
W_C	net channel thickness
W	channel width
W_B	epitaxial-layer thickness
W_{CIB}	current-induced basewidth
X_A	channel thickness of the MOSFET
$X_{A(min)}$	minimum channel thickness of the MOSFET
X_d	depletion-layer width
X_i	depth of the accumulation layer from the surface
X_j	junction depth of channel diffusion
X_B, X_{dn}	depletion-layer width on the channel side
Z	width of the resistive element

α	spreading angle
α_o	product of emitter efficiency and the base transport factor
β	common-emitter current gain gain factor of the MOS transistor [= (W/L) μC_o]
γ	MOS-transistor bulk-charge factor
ε_{ox}	permittivity of SiO_2
ε_{si}	permittivity of Si
Θ	600°K
μ	hole bulk mobility
μ_n	electron bulk mobility
$\hat{\mu}$	average hole bulk mobility
μ_E	electron inversion-layer mobility
μ_D	electron accumulation-layer mobility
μ_{eff}	effective mobility
μ_{FE}	field-effect mobility
μ_{max}	maximum value of effective mobility
ρ	resistivity
ρ_s	sheet resistivity
σ	conductivity
ϕ_B	built-in potential
ϕ_c	voltage across the depletion layer on the channel side
ϕ_d	voltage across the depletion layer on the epitaxial-layer side
ϕ_F	Fermi level referenced by midgap
ϕ_{ms}	metal semiconductor work-function difference
χ_e	semiconductor electron affinity
χ_m	metal electron affinity (work function)
ψ_s	surface potential

τ_E	emitter delay
τ_B	base transit time
τ_{sc}	space-charge generation lifetime
τ_n	minority-carrier lifetime

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Chapter I

INTRODUCTION

Until recently, silicon bipolar transistors were the principal active components for power amplification and switching applications because of high current density and good geometrical control of the active transit (base) region width. Recent advances in processing technology and the introduction of new device structures, however, have dramatically improved the current, voltage, and power-handling capabilities of MOSFETs. The impetus for much of this work is the faster switching ability of majority-carrier devices which are not affected by the minority-carrier charge-storage problems inherent in bipolar transistors. A second motivation is the negative temperature coefficient of carrier mobility that greatly reduces the problems of thermal runaway, secondary breakdown, and current hogging—all play important roles in the design and application of power bipolar transistors. The recent commercial availability of a variety of discrete power MOS transistors has made possible numerous new applications.

The power-frequency performance of various semiconductor devices is illustrated in Fig. 1.1 [1.1]. As technology continues to develop, new

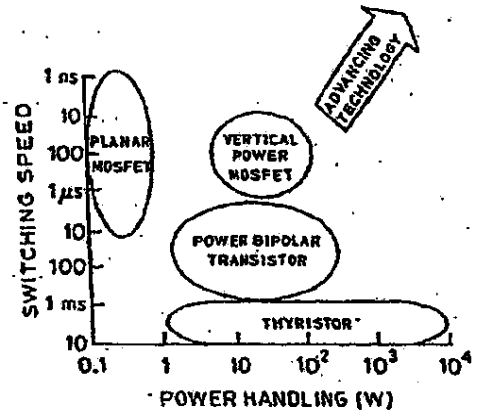

Fig. 1.1 SPEED VS POWER IN VARIOUS SEMICONDUCTOR DEVICES.

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limits on the power-handling capability and switching speed will be established. It can be seen that the trends are moving upward toward the right.

The thyristor is a bistable solid-state device that blocks the flow of current until it is turned on by a small control signal; it then remains on until the supply voltage is removed or reversed in polarity. Although these devices are able to control large amounts of power, they are usually limited to switching frequencies of only a few kilohertz.

The bipolar power transistor functions in the same way as its small-signal counterpart, but it is large enough to control power levels up to several hundreds of watts. A continuous base current is required to maintain this device in the on-state, and this power is lost and detracts from the efficiency of the transistor as a switch. Although it is capable of switching at a much higher rate than the thyristor, time delays associated with the injection and removal of base charge limit its switching speed to less than 20 kHz.

The planar MOSFET requires a negligible amount of power to control the switching action because it is a voltage-controlled device. Lacking the time delays inherent in a bipolar transistor, the planar MOSFET can be operated at frequencies up to hundreds of megahertz; unfortunately, however, the current to be controlled is conducted laterally through a relatively long channel. The resulting high on-resistance limits the use of this MOSFET to power-handling applications of ≤ 1 W.

In the newly developed vertical power MOSFET, drain current is collected from the substrate which obviates the need for a drain-contact area on the surface. The resulting increase in packing density directly reduces the cost and improves the performance of the device. In this vertical structure, the best features of earlier technologies and innovative design are combined with new fabrication techniques to achieve performance that can be an order of magnitude better than previously attainable.

A. Major Modifications in Power MOSFETs

Two modifications in the basic MOSFET structure have been responsible for the advancements in the current-handling capability and breakdown

voltage. The first is the use of double diffusion to achieve very short (1 to 3 μ) channels [1.2,1.3] although not all of the new power MOSFETs use this technique [1.4]. Sequential diffusion of P- and N-type impurities in a manner analogous to bipolar-transistor fabrication processes yields channel lengths comparable to bipolar basewidths. Historically, this process has been difficult to control because threshold voltage is determined by diffused impurity profiles rather than by bulk substrate doping levels. Ion implantation, however, has largely resolved this problem.

The second major change has been the incorporation of a lightly doped (usually N^-) drift region between the channel and the N^+ drain contact [1.2-1.5]. This region largely supports the applied drain potential because its doping level is much smaller than the P-channel region. These new structures effectively separate the active channel (which determines device gain) from the drift region that supports the applied voltage. This separation is identical in modern bipolar transistors where a lightly doped collector region supports the applied potential and a narrow and more heavily doped base region determines device gain.

Table 1.1 lists the principal differences and similarities between power MOS and bipolar transistors. In addition to their inherent high switching speed resulting from the lack of minority-carrier injection during operation, MOSFETs with their insulated gates have negligible input gate-drive current; other advantages are related to the negative temperature coefficient of their drain current, which prevents the formation of thermal instabilities and simplifies the paralleling of devices to increase current handling. In contrast, bipolar transistors require ballasting and careful device matching to prevent thermal runaway.

At lower frequencies, MOSFET on-resistance is higher than in bipolar transistors rated at the same operating voltage. This results in larger steady-state power dissipation and may offset the advantages. The prospects for commercial power MOSFETs appear bright, however, in many high-frequency applications.

Table 1.1

COMPARISON OF MOS AND BIPOLAR POWER TRANSISTORS

MOS	Bipolar
Differences	
Majority-carrier device	Minority-carrier device
no charge-storage effects	charge stored in the base and collector
high switching speed	low switching speed
drift current (fast process)	diffusion current (slow process)
Voltage driven	Current driven
purely capacitive input impedance; no dc current required	low input impedance; dc current required
simple drive circuitry	complex drive circuitry (resulting from high base-current requirement)
Predominantly negative temperature coefficient on drain current	Positive temperature coefficient on collector current
no thermal runaway	thermal runaway
devices can be paralleled	devices cannot be easily paralleled because of V_{BE} matching problem and local current concentration
Less susceptible to second breakdown	Susceptible to second breakdown
Square-law I-V characteristics at low current; linear I-V characteristics at high current	Exponential I-V characteristics
Greater linear operation and fewer harmonics	More intermodulation and cross-modulation products
High on-resistance and, therefore, larger conduction loss	Low on-resistance (low saturation voltage) because of conductivity modulation of high-resistivity drift region
Low transconductance	High transconductance
Turn-on voltage directly affected by such process parameters as doping profiles	Turn-on voltage relatively insensitive to process parameters

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Table 1.1

CONTINUED

Similarities	
Channel length determined by double diffusion	Basewidth determined by double diffusion
Drain current proportional to channel width	Collector current approximately proportional to emitter stripe length
High breakdown voltage as the result of a lightly doped region of a channel-drain blocking junction	High breakdown voltage as the result of a lightly doped region of a base-collector blocking junction

B. Commercial Power MOSFETs

Although most of the recently developed power MOSFETs are based on the two modifications described in Section A, there are substantial variations in the structures used to implement them. A host of commercial MOSFET devices has entered the industrial market; they are known by such names as VMOS [1.6], DMOS [1.2], HEXFET [1.7], TMOS [1.8], and SIPMOS [1.9]. These products, however, can be described by three basic structures--the lateral double-diffused transistor (LDMOS) [1.2], vertical double-diffused transistor (VDMOS) [1.10], and V-groove double-diffused transistor (VMOS) [1.6]. The selection of the appropriate device will depend on the voltage, current, power, and speed requirements for a specific application.

In late 1978, International Rectifier developed the HEXFET (Fig. 1.2) which was a refinement of the generic silicon-gate VDMOS, with the capability of handling up to 400 V at 5 A continuous current. Since then, Motorola with its TMOS (Fig. 1.3) and Siemens with its SIPMOS (Fig. 1.4) have joined the competition. Recently, RCA has introduced a structure similar to the HEXFET. Table 1.2 is a partial list of some of the major manufacturers and their products.

Despite all of this commercial activity, there are few theoretical analyses of device capabilities and comparisons of the various structures.

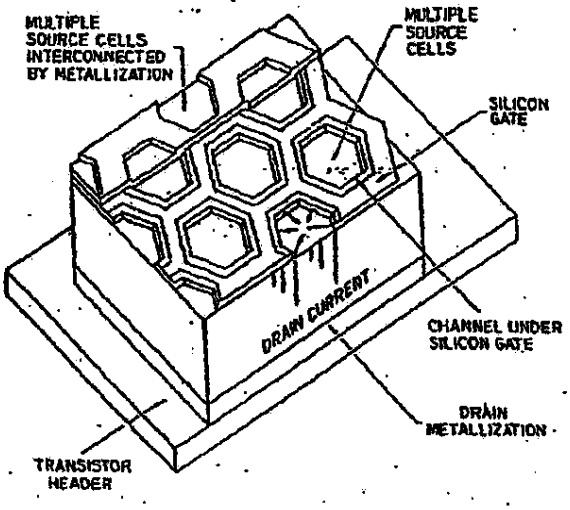


Fig. 1.2. THE HEXFET.

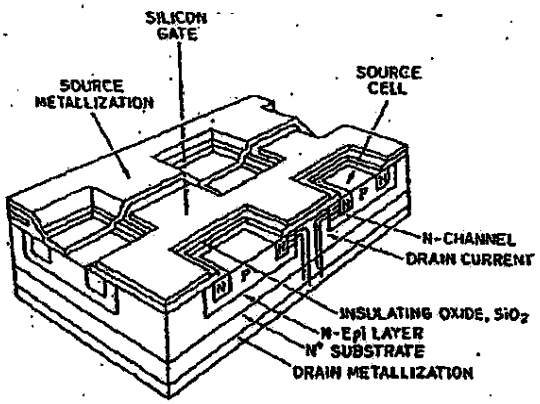


Fig. 1.3. CROSS SECTION OF THE MOTOROLA TMOS POWER FET. This structure is based on the VDMOS.

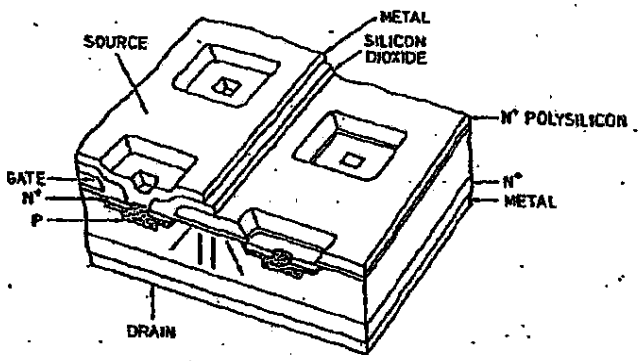


Fig. 1.4. SIEMENS POWER MOSFET (SIPMOS)—A VARIATION OF THE VDMOS.

Table 1.2

COMMERCIAL POWER MOSFETs AND THEIR MANUFACTURERS†

Manufacturer	Voltage Rating (V)	Technology
Hewlwett-Packard	450	VDMOS
Supertex	450	VDMOS
International Rectifier	500/400	VDMOS
Motorola	500/400	VDMOS
Intersil	800, 700, 450	VDMOS
Siemens	100	VDMOS
T.I.	80, 90	VMOS
Siliconix	90, 450	VMOS
General Electric	450, 300	VMOS

†Obtained from manufacturer data sheets, advertisements, or technical reports and publications.

This lack of published data has supplied the motivation for the work reported here. Its purpose is to investigate the physics and technology of power MOSFETs and to determine the key parameters in device modeling.

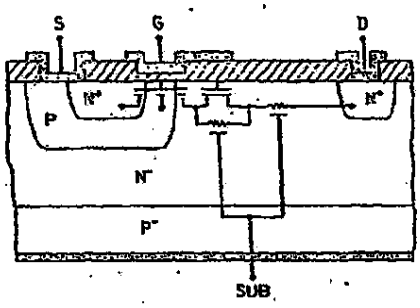
D. Organization

Chapter II begins with a brief introduction to the power MOSFETs, followed by equivalent-circuit representations. Quantitative models, suitable for device design, are developed directly from the geometry and doping profiles to determine the on-resistance of each device. These models are useful in optimizing a particular structure and in comparing all of them for a specific application. Test structures have been fabricated to evaluate performance and to verify the accuracy of the models. A VDMOS with a hexagonal geometry is illustrated, using the analytical model to optimize the on-resistance. The dc I-V characteristics are investigated, with emphasis on the VDMOS. Transconductance and its limitations resulting from the operating conditions and geometries are analyzed.

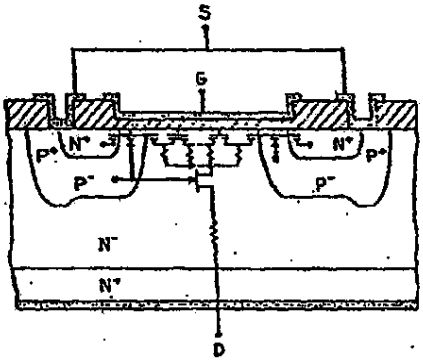
Voltage limitations and the parasitic bipolar effect intrinsic in power MOSFETs are considered in Chapter III. A modified figure of merit for the voltage-frequency relationship is introduced. The fundamental differences in frequency response and on-resistance between MOS and bipolar devices are analyzed.

Knowledge of electron mobility in the inversion and accumulation layers is essential for accurate modeling of the power MOSFETs described in Chapter II because it is a key parameter in determining device performance. The need for accurate mobility data motivated the mobility measurements and data analysis, and the results are described in Chapter IV.

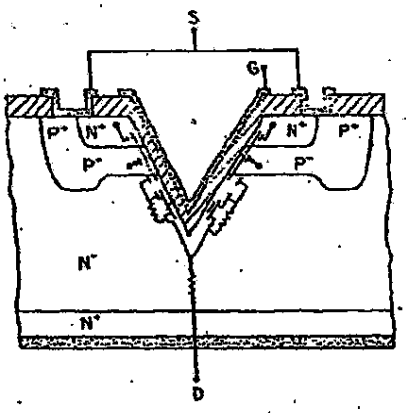
Discrete power MOSFETs have advanced rapidly during the last few years; however, there is also an increasing interest in integrated circuits with a portion of their circuitry operating at high voltages. A new development in the lateral DMOS is the use of a thin-epitaxial layer, and this is discussed in Chapter V. Key device parameters are identified through both analytical solutions and two-dimensional numerical simulations.



a. LDMOS



b. VDMOS



c. VMOS

Fig. 2.1. CROSS SECTIONS OF THREE HIGH-VOLTAGE DMOS DEVICES.

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than the LDMOS whose drain connection is on the top surface. Most power MOSFETs manufactured today use one of the vertical structures for this reason. The LDMOS, however, has the advantage of much simpler integration with other components [2.3] because all three electrodes are on the top surface and are readily available for interconnection to other devices. In addition, in lower voltage applications in which the LDMOS gate electrode may be extended all the way to the drain N^+ region over thin oxide [2.4], the gate potential can reduce the resistance of the N^- drift region substantially by heavily accumulating the surface. This mechanism cannot occur in the vertical structures, and it makes the LDMOS more competitive in current per unit area with the vertical devices at low voltages.

Both the LDMOS and VDMOS can be fabricated on any silicon-crystalline orientation. The VMOS channel is constrained along an etched <111> surface. The choice of <100> material for the LDMOS and VDMOS results in a 20 percent improvement in electron inversion-layer mobility [2.5, 2.6] and a 15 percent improvement in inversion-layer electron scattering-limited velocity v_{SAT} [2.7]. These effects lower channel resistance and increase device transconductance per unit width in the LDMOS and VDMOS.

The fixed oxide charge density Q_f is approximately three times greater on the <111> plane than it is on the <100> plane [2.8]. For a given threshold voltage, therefore, peak channel doping must be higher in the VMOS structure than it is in the LDMOS or VDMOS. Because electron inversion-layer mobility decreases with increased doping [2.5,2.6], this would again imply greater mobility in the LDMOS and VDMOS. In practice, however, this effect is negligible in higher voltage devices because channel doping in all three structures is heavy enough for the bulk-charge term to dominate the threshold voltage, with little contribution from Q_f [2.9]. The higher Q_f in the VMOS, however, may degrade mobility [2.5,2.10], and it generally implies a greater interface state (N_{it}) density that may impact other device parameters such as noise performance in linear-amplification applications [2.11].

The nonplanar VMOS can encounter fabrication difficulties in terms of metal coverage and photolithography which do not exist in the planar

LDMOS and VDMOS. The increasing use of silicon-gate technologies in the fabrication of all three types, however, has largely eliminated this potential problem.

All three structures inherently have some overlap of the thin gate oxide over the heavily doped N^+ source region. This contributes directly to gate-to-source capacitance C_{GS} and degrades the speed of the devices. In metal-gate technologies, this capacitance can be reduced substantially by making use of the differential oxidation rates over the N^+ and N^- regions [2.12]. Such techniques are more effective on <100>-oriented silicon than on <111> substrates, and this would tend to favor the LDMOS and VDMOS when high-frequency performance is required. In addition, implementation of self-aligned silicon-gate technology is relatively straightforward in the planar devices; it is not as effective in reducing C_{GS} in the VMOS.

In high-voltage applications, the bulk resistance of the N^- region in each device plays a major role in overall on-resistance, as will be demonstrated quantitatively in Section E. The three structures inherently have such a bulk resistance; however, the values vary. Equivalent circuits for the LDMOS, VDMOS, and VMOS are examined in the following section to pinpoint the differences in this component in each structure.

B. Equivalent Circuits

The equivalent circuits of the LDMOS, VDMOS, and VMOS are presented in Fig. 2.2. Each structure consists basically of an enhancement-mode transistor in series with a parasitic bulk resistance; however, a more careful examination of these circuits will reveal some basic differences.

The LDMOS (Fig. 2.2a) consists of an enhancement-mode transistor (active channel) in series with a depletion-mode transistor (surface accumulation region) which is in parallel with a bulk resistor R_1 in series with a second bulk resistor R_2 [2.13]. The two components in the center represent the gate-controlled accumulation layer in parallel with a bulk resistor; the current through the device will divide between these two components in a manner determined by the conductance of the accumulation layer (gate voltage). The third series component R_2 represents the region between the gate electrode and drain contact; such a

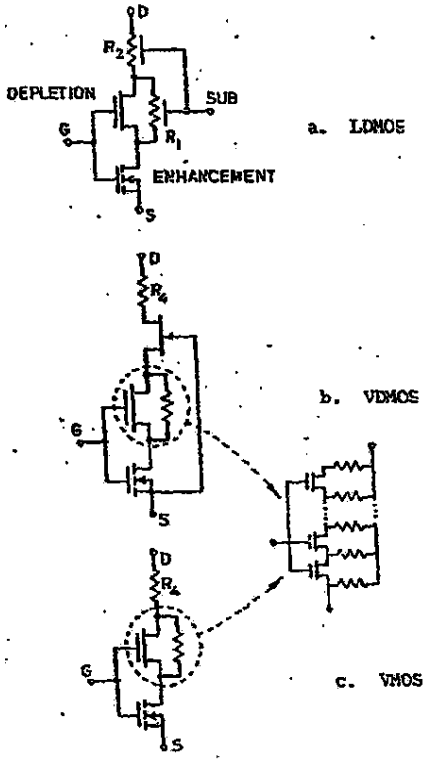


Fig. 2.2. EQUIVALENT CIRCUITS OF HIGH-VOLTAGE DMOS DEVICES.

region would be missing in a low-voltage structure in which the gate metal could extend to the N^+ region [2.4]. In a junction-isolated device, the substrate PN^- junction modulates the conductivity of R_1 and R_2.

The VDMOS (Fig. 2.2b) is distinguished from the LDMOS in two ways. First, the depletion-mode transistor and its parallel bulk resistor must be regarded as distributed devices because the direction of current flow changes from horizontal to vertical along the length of the accumulated surface between the source regions. The distributed model will be simplified here to a single depletion-mode transistor; a correction factor

will be introduced in Section E to account for the two-dimensional nature of current flow. Second, a series JFET is present in the equivalent circuit of the VDMOS because of the pinching of current between the adjacent P-bulk diffusions. The spacing between the P diffusions (channel width of the JFET) can be a significant factor in determining the fraction of total on-resistance contributed by the series JFET.

The VMOS equivalent circuit (Fig. 2.2c) is identical to that of the LDMOS except for the absence of any influence of a P-type substrate on R_1 and R_2 because the VMOS is regarded here as a nonisolated discrete device. The physical structure of the VMOS, however, varies distinctly from the LDMOS and, as a result, analyses of the components in the two models will differ for each.

To simplify the analyses of the three devices based on these equivalent circuits, two-dimensional distributed structures are reduced to lumped equivalent circuits. With minor geometrical corrections to account for this modification, the models in Fig. 2.2 are in good agreement with a variety of experimental structures.

Even with the above simplifications, modeling of these devices is not straightforward for the following reasons.

- Because each of the enhancement-mode devices in Fig. 2.2 has a nonuniformly doped channel, electron inversion-layer mobility and scattering-limited velocity variations with doping must be known as should their variation with the gate field.
- Depletion-mode devices are present in each circuit (representing surface-accumulation layers). Electron (majority-carrier) mobility in such regions must also be known, therefore, including its dependence on the gate field.
- The bulk resistors in each circuit are two dimensional and, as a result, realistic geometries for these regions must be developed.

C. Device Design

To investigate the accuracy of the models in Fig. 2.2 and the analytical expressions to be presented in Section E, the three devices were fabricated side by side on the same wafer. Figure 2.3 is a

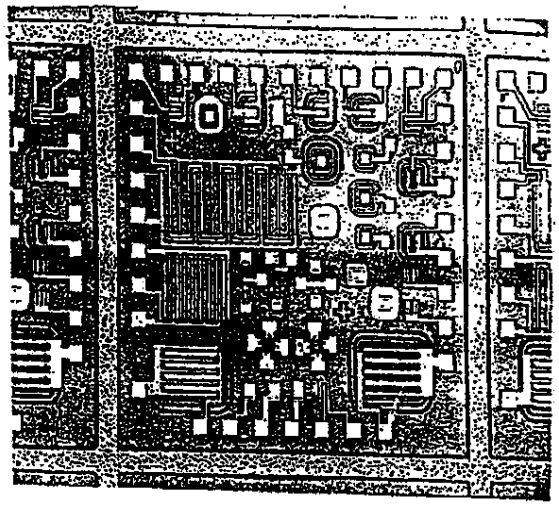
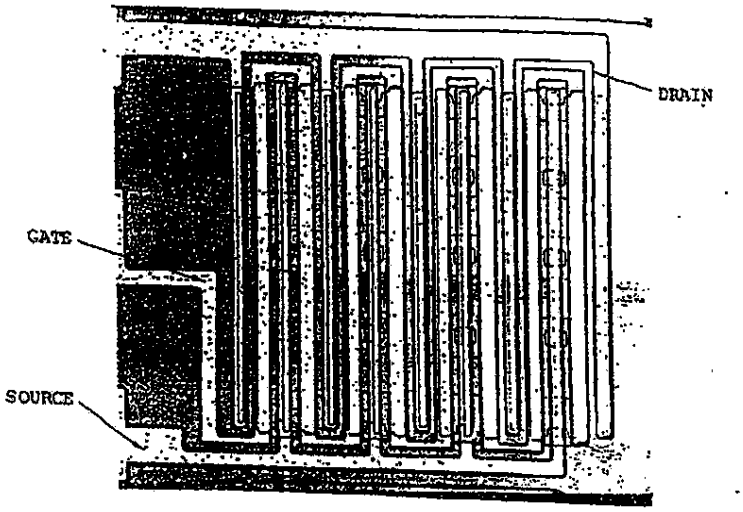


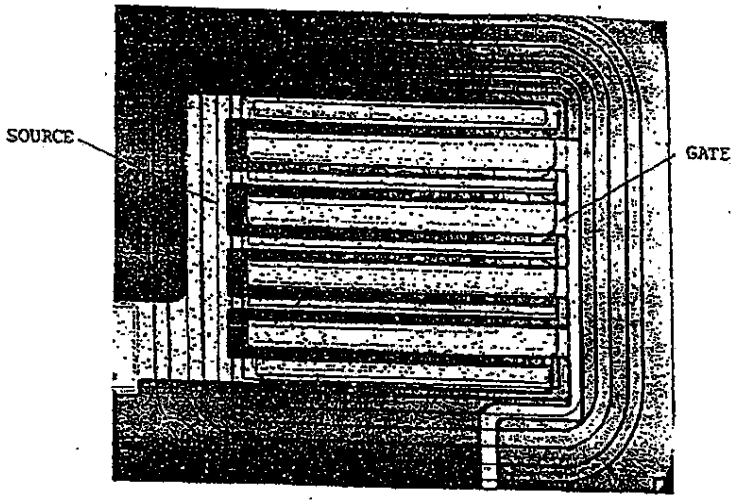
Fig. 2.3. PHOTOMICROGRAPH OF THE POWER-MOSFET TEST CHIP.

photomicrograph of the completed power-MOSFET test chip. Design rules were 10 μ minimum feature sizes and 5 μ alignment tolerances, and the resulting photomicrographs (from the same die) at a larger magnification are presented in Fig. 2.4. The channel width of each device was 3440 μ, and the channel lengths were determined from the spreading-resistance measurements of the vertical profile and 85 percent conversion from vertical to lateral distances. These parameters are listed in Table 2.1. Epitaxial thicknesses were obtained by the commonly used lap-and-stain technique. Diffused guard rings were employed to prevent the surface effects from degrading the breakdown voltage [2.14]. Such techniques are not as easily employed in the LDMOS because of its topside drain contact and, as a result, they were not used for the structure in Fig. 2.4a.

Because the area occupied by each device is highly dependent on design rules and voltage capability, each device was developed according to the same design rules and had a voltage capability of >300 V in the highest resistivity epitaxial material (8.5 Ω-cm). For the same total

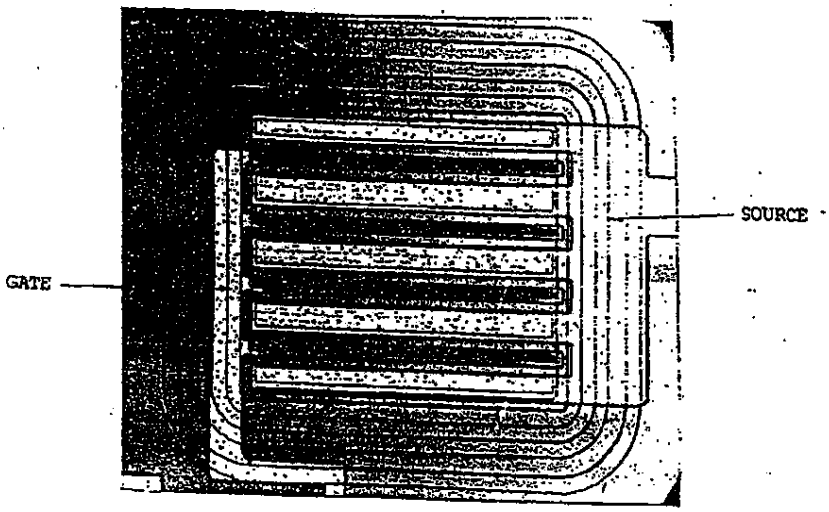


a. LDMOS



b. VDMOS

Fig. 2.4. PHOTOMICROGRAPHS OF THE HIGH-VOLTAGE DMOS DEVICES WITH IDENTICAL CHANNEL WIDTHS FABRICATED ON THE SAME WAFER.



c. VMOS

Fig. 2.4. CONTINUED.

Table 2.1

EXPERIMENTAL PARAMETERS FOR FABRICATED DEVICES

Wafer Resistivity (Ω-cm)	Effective Epitaxial Thickness between P Diffusion and N^+ Substrate (μ)	LDMOS, VDMOS L_{eff} (μ)	VMOS L_{eff} (μ)
0.5	6.4	1.50	2.17
1.1	7.3	1.62	2.34
3.0	14.6	1.79	2.58
7.0	20.3	2.00	2.88
8.5	26.8	2.13	3.06

channel width, the relative surface areas excluding guard rings were 1.62, 1.08, and 1.0 for the LDMOS, VDMOS, and VMOS, respectively. A more important criterion than surface area for a given channel width, however, is surface area for a given on-resistance or current capability as will be discussed in Section E.

Small VDMOS structures with various spacings between the p-wells were included on the same die to determine the effect of the JFET component (Fig. 2.2) on the on-resistance. Two small VMOS devices with different spacings in the V-groove opening were used to study the V-groove depth and incomplete V-groove etch effects. To extend the breakdown voltages, several types of junction-edge termination techniques (such as p-type field-limiting rings and field plates) were also included on the chip. The Van der Pauw patterns facilitated the measurement of the sheet resistances.

D. Epitaxial-Layer Resistivity and Thickness

In high-voltage structures, on-resistance is dominated by the bulk resistance of the drift region. For this reason, the thickness and resistivity of the epitaxial layer must be carefully chosen for optimal device performance. These parameters are examined in this section, based on a simple one-dimensional model (inset in Fig. 2.5) in which the N^- region represents the epitaxial layer with thickness W_B between the topside P diffusion and N^+ substrate and doping density N_D.

On-resistance is minimized when the source-drain depletion region is allowed to spread completely through the epitaxial layer. Under this punchthrough condition, the voltage capability of the device is limited by avalanche breakdown when the field in the depletion region reaches the critical electric field E_{crit}. For abrupt junctions and neglecting the built-in potential, the depletion-layer width W_B [2.15] is

$$W_B = \sqrt{\frac{2\varepsilon_{si} BV}{qN_D}} \qquad (2.1)$$

where

ε_{si} = dielectric permittivity of silicon = 1.04×10^{-12} F/cm

BV = breakdown voltage

q = electric charge = 1.6×10^{-19} coul

N_D = donor impurity concentration (cm^{-3})

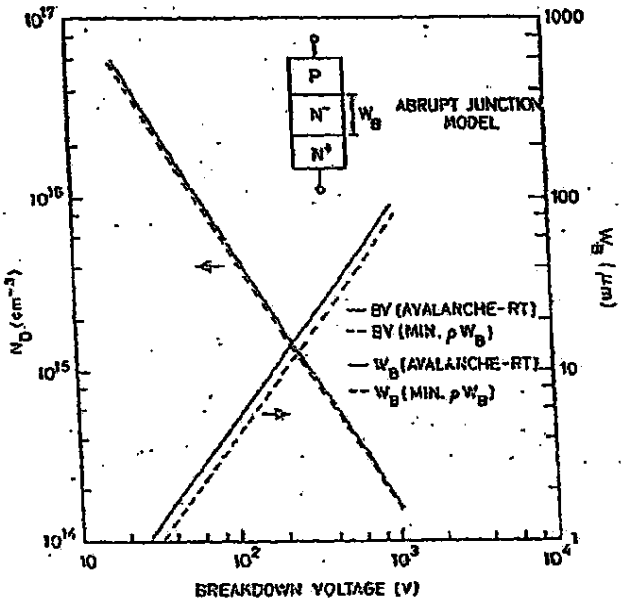


Fig. 2.5. EPITAXIAL-LAYER DOPING CONCENTRATION AND THICKNESS VS BREAKDOWN.

Based on the data in Ref. 2.16 and listed in Table 2.2, an approximate expression for the dependence of a plane-junction avalanche breakdown voltage on doping can be obtained as

$$BV \cong 2.932 \times 10^{12} N_D^{-0.666} \text{ V} \qquad (2.2)$$

Simultaneous solutions of these two equations yield the solid lines in Fig. 2.5 which indicate the required W_B and N_D as a function of the

Table 2.2

BREAKDOWN-VOLTAGE DEPENDENCE OF DOPING CONCENTRATION ON AN ABRUPT PLANE JUNCTION

Doping Concentration N_D (cm^{-3})	Breakdown Voltage from Ref. 2.16 (V)	Breakdown Voltage from Eq. (2.2) (V)
1×10^{14}	1400	1390.5
1×10^{15}	300	300
1×10^{16}	63	64.7
1×10^{17}	14.5	14

desired punchthrough-limited breakdown voltage. Note that, at this breakdown voltage, the depletion region just reaches the n^-/n^+ interface.

The above formulation does not completely reduce the on-resistance. A better approach is to minimize the product ρW_B which is proportional to the bulk series resistance of each device; that is, for a given BV requirement,

$$\frac{\partial}{\partial N_D}(\rho W_B) = 0 \tag{2.3}$$

where ρ is the epitaxial-layer resistivity defined as

$$\rho = \frac{1}{qN_D\mu(N_D)} \tag{2.4}$$

where $\mu(N_D)$ is the bulk electron mobility.

The empirical formulation by Caughey and Thomas [2.17] for $\mu(N_D)$ is

$$\mu(N_D) = \frac{\mu_{MAX} - \mu_{MIN}}{1 + (N_D/N_{REF})^{\alpha}} + \mu_{MIN} \tag{2.5}$$

where μ_{MAX} and μ_{MIN} are the limiting values of the bulk electron mobility in lightly and heavily doped material, respectively (μ_{MAX} = 1330 $cm^2/Vsec$, μ_{MIN} = 65 $cm^2/Vsec$), $N_{REF} = 8.5 \times 10^{16}$, and $\alpha = 0.72$.

Under the reachthrough condition, the epitaxial-layer thickness W_B can be obtained from Ref. 2.18 as

$$BV_{RT} = E_{crit} W_B - \frac{qN_D W_B^2}{2\epsilon_{si}} \qquad (2.6)$$

where BV_{RT} is the reachthrough-limited breakdown voltage and differs from the voltage derived in Eq. (2.2). This becomes more apparent when the electric-field configuration in Fig. 2.6 is examined: here, Fig. 2.6a is based on Eq. (2.2) and Fig. 2.6b is according to Eq. (2.6).

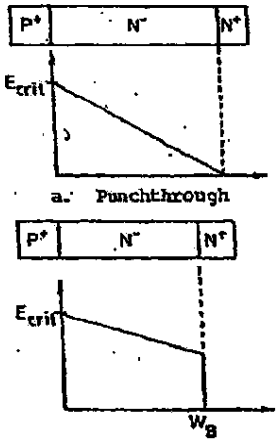


Fig. 2.6. ONE-DIMENSIONAL ELECTRIC FIELD.

To determine the doping dependence of E_{crit}, Eq. (2.2) is substituted [2.15] into

$$E_{crit} = \left(\frac{2qN_D BV}{\epsilon_{si}}\right)^{1/2} \qquad (2.7)$$

and the critical electric field then becomes

$$E_{crit} = \sqrt{(2qN_D/\epsilon_{si})(2.932 \times 10^{12} N_D^{-0.666})} \qquad (2.8)$$

which, when substituted into Eq. (2.6) and solving for W_B yields

$$W_B = \sqrt{\frac{2\epsilon_{si}}{qN_D}}\left(\sqrt{2.932 \times 10^{12} N_D^{-0.666}} - \sqrt{2.932 \times 10^{12} N_D^{-0.666} - BV_{RT}}\right) \qquad (2.9)$$

Combining Eqs. (2.4) and (2.5) for ρ and Eq. (2.9) for W_B in (2.3), the ρW_B product becomes a function of N_D only.

The optimal values of N_D and W_B that minimize epitaxial bulk resistance are thereby obtained, and the results are plotted (dashed lines) in Fig. 2.5. These values are not substantially different from those indicated by the solid lines; they do imply, however, that less doping and a reduction in the thickness of the epitaxial layer will lower the on-resistance as compared to a direct calculation based only on Eqs. (2.1) and (2.2). In actual practice, the degree of control that can be achieved over epitaxial-layer thickness and doping and the need to allow for process tolerances make the differences between the solid and dashed curves a second-order consideration.

Figure 2.7 plots the results of the calculation of ρW_B as a function of W_B and the corresponding N_D for a 300 V device. At BV = 300 V, the depletion-region width at the N^- side is 20 μ and any W_B greater than 20 μ will contribute unnecessary on-resistance. A 300 V breakdown voltage can be maintained, however, if both W_B and N_D are reduced because of the dependence of E_{crit} on the doping concentration. Below the minimum ρW_B point, any further drop in W_B will increase the on-resistance. For any required BV, a similar calculation can yield optimal values for ρ and W_B.

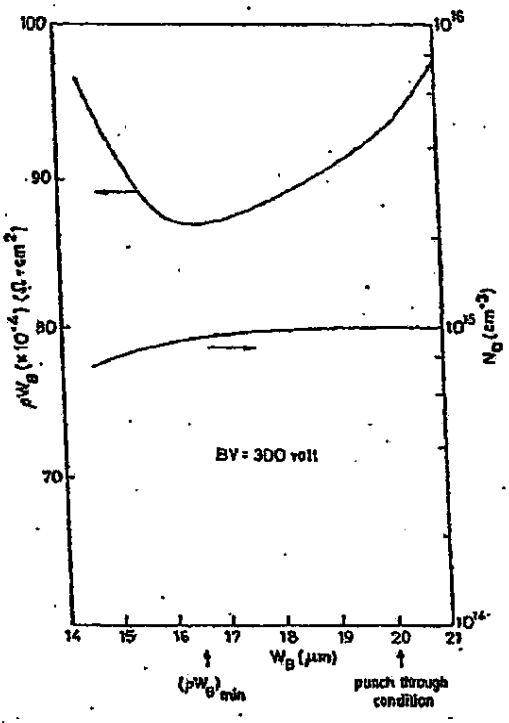


Fig. 2.7. PRODUCT OF RESISTIVITY AND THICKNESS OF THE EPITAXIAL LAYER ρW_B. This is a measure of the epitaxial contribution to on-resistance vs net epitaxial thickness W_B and doping concentration N_D for a 300 V device.

E. Modeling of Device On-Resistance

1. LDMOS

The LDMOS equivalent circuit (Fig. 2.2a) contains four components. In high-voltage structures, however, the lateral extent of the thin gate oxide over the N^- drift region and the lateral extent of the metal gate after it steps up over the thick oxide above the N^- drift region (Fig. 2.1a) are generally small compared to the total extent of the N^- region [2.3]. This configuration is necessary to maximize the voltage capability of the device because the gate metal serves as a

field plate [2.3,2.4]. As a result, the contributions of the depletion-mode device and bulk resistor R_1 to total on-resistance are normally small and, therefore, the contribution of the depletion-mode device can be neglected and only R_1 is included in the calculation of R_2. In low-voltage structures in which this is not a valid approximation, the formulations in Sections E.2 and E.3 for the VDMOS and VMOS can be directly extended to the LDMOS. With this simplifying assumption, the equivalent circuit becomes an enhancement-mode transistor in series with a bulk resistor.

Based on the assumptions of small drain-source bias and uniform channel doping, the enhancement-mode channel resistance becomes

$$R_E = \frac{1}{(W/L_{eff})\, C_o \mu_E(V_G)(V_G - V_{TE})} \qquad (2.10)$$

where

W = channel width

L_{eff} = effective channel length

C_o = gate-oxide capacitance/unit area

$\mu_E(V_G)$ = electron inversion-layer mobility

V_{TE} = threshold voltage of the enhancement-mode device

For the LDMOS whose photomicrograph is shown in Fig. 2.4a, $W = 3440\ \mu$ and $L_{eff} \cong 85$ percent of the vertical difference in the N^+ and P diffusion depths. For the same diffusion schedules, L_{eff} will depend on the epitaxial-layer concentration (Table 2.1) because the PN^- junction depth depends on N^- doping. Here, C_o was obtained directly from the measured gate-oxide thickness of 950 Å, and V_{TE} was determined to be +2 V. Electron inversion-layer mobility depends on channel doping. In the devices considered here, $N_{A_{MAX}} = 5 \times 10^{16}/cm^3$ and, therefore, $\mu_{E_{MAX}} \cong 560\ cm^2/Vsec$ [2.5,2.6]. As gate bias is applied, the effective mobility will be reduced because of the vertical component of the electric field existing in the channel. In the calculation of on-resistance, the data in Refs. 2.5 and 2.19 were used to account for this reduction.

To model the bulk resistor R_2 in the LDMOS equivalent circuit, current is considered to flow from a line source with radius r_1 at the end of the channel to a line sink with radius r_2 at the N^+ contact (Fig. 2.8). This model is analogous to the electrostatic problem of an image charge in a conducting plane [2.20] and has been analyzed in detail by Pocha [2.13] who reported that the resulting resistance of the bulk epitaxial region is

$$R_2 = \frac{\rho}{W\pi}\left[\ln\left(\frac{L' - r_1}{r_1}\right) + \ln\left(\frac{L' - r_2}{r_2}\right)\right] \qquad (2.11)$$

where

L' = effective length of the N^- epitaxial resistor

r_1 = effective radius of the current source at the end of the channel

r_2 = effective radius of the current sink at the N^+ contact

Here, $L' \approx 24\ \mu$ was obtained directly from the mask dimensions of the device and the extent of the lateral diffusion of the P channel and N^+ diffusions; r_1 is related to the effective "emitting" area at the end of the channel ($r_1 = 0.5\ \mu$ was in reasonable agreement with experiment), and r_2 is related to the effective "collecting" area of the N^+ diffusion ($r_2 = 2\ \mu$, close to the N^+ junction depth, was in good agreement in the devices considered here).

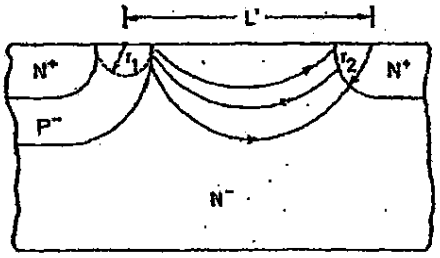


Fig. 2.8. MODEL OF THE LDMOS USED TO CALCULATE BULK RESISTANCE.

From the above formulations for R_E and R_2, the calculated results plotted in Fig. 2.9 were compared to the experimental results obtained at three epitaxial-layer resistivities (see Table 2.1 for epitaxial thicknesses and L_{eff} values). The drain voltage was limited to <100 mV to hold the devices in their linear region of operation.

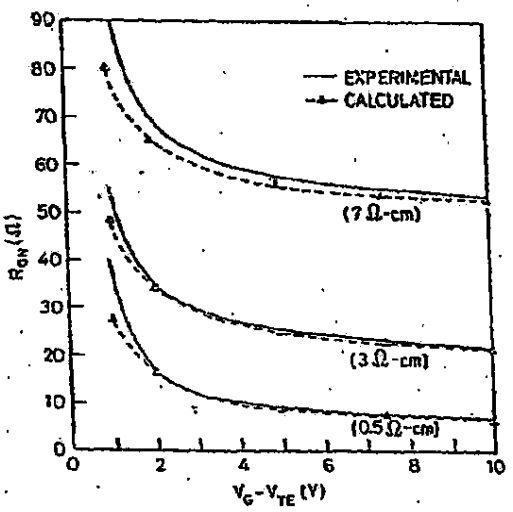


Fig. 2.9. ON-RESISTANCE OF LDMOS DEVICES VS $V_G - V_{TE}$.

The agreement between these calculated and experimental results is good except for the gate-voltage values close to the threshold. There are two reasons for this discrepancy. First, in this region, channel resistance R_E dominates and the inaccuracies in Eq. (2.10) become important because, for example, this expression does not take into account the nonuniform-channel doping profile; more accurate models [2.21] could possibly reduce this error. Second, under moderate to high gate biases, the thin-oxide overlap of the N^- region creates a surface accumulation layer that helps to prevent current crowding at the end of the channel; as the gate bias is reduced, this crowding becomes more severe (r_1 decreases) which leads to higher on-resistance than predicted

by the models. Whatever the reason, the small errors at low V_G are not critical in many applications of power MOSFETs because gate voltages substantially above V_{TE} would be used. The contributions of R_E and R_1 to overall on-resistance will be considered specifically for the VDMOS in the following section.

2. VDMOS

Calculation of on-resistance in the VDMOS is illustrated in Fig. 2.10a and, for clarity, Fig. 2.10b is the top view of the VDMOS "cell." The thin gate oxide normally extends all the way between the adjacent source and channel diffusions. As a result, the surface accumulation layer (region ②) plays an important role in total on-resistance and cannot be neglected; physically, it collects the channel current and distributes it over the region between adjacent P diffusions, thereby preventing current crowding at the end of the channel and helping to reduce the on-resistance. This behavior is expected to be most effective at high gate voltages that maximize the conductivity of the accumulation layer. This has been confirmed by a rigorous two-dimensional computer simulation [2.22] in which the electron current was observed to flow uniformly and vertically toward the drain from the accumulation layer.

In addition, a junction field-effect transistor exists between the adjacent P diffusions (Fig. 2.2b). Depending on its ratio of channel width to P diffusion depth, this JFET can also play a significant role in overall on-resistance.

Neglecting contact resistances and the resistance of the bulk N^+ substrate, the VDMOS on-resistance is

$$R_{ON_{VDMOS}} = R_E + R_D + R_{JFET} + R_d \qquad (2.12)$$

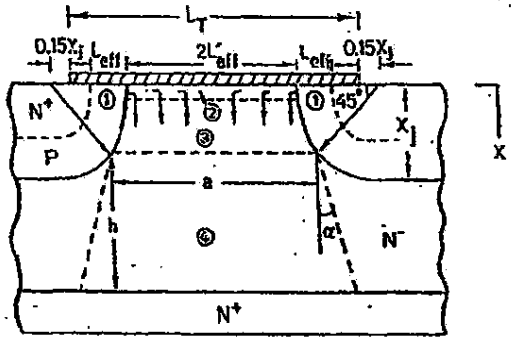
where

R_E = enhancement-mode on-resistance [the same as in Eq. (2.10), used in modeling the LDMOS]

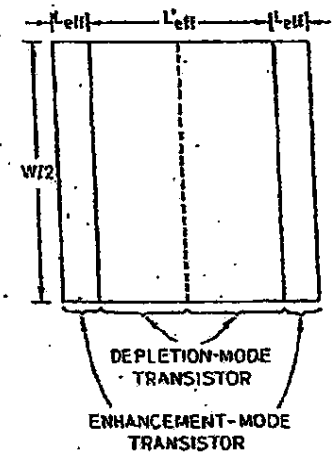
R_D = depletion-mode on-resistance (surface accumulation layer)

R_{JFET} = JFET on-resistance

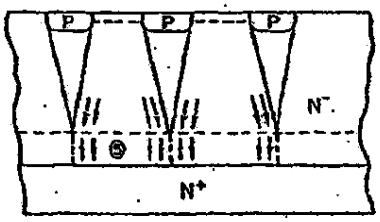
R_d = bulk epitaxial-layer resistance



a. Separation into four series components with parameter definitions



b. Top view of the VDMOS "cell"



c. Modification to account for overlapping of bulk epitaxial trapezoids

Fig. 2.10. MODEL OF THE VDMOS USED TO CALCULATE ON-RESISTANCE.

The parameters in R_E are the same as those for the LDMOS. As shown in Fig. 2.10b, $W/2$ is the channel on one side of the cell and W denotes the total channel width.

The following expression for the depletion-mode on-resistance is analogous to Eq. (2.10):

$$R_D = \frac{1}{3} \frac{1}{(W/L'_{eff}) C_o \mu_D(V_G)(V_G - V_{TD})} \tag{2.13}$$

where $\mu_D(V_G)$ is electron (majority-carrier) accumulation-layer mobility and L'_{eff} is the effective depletion-mode channel length. The factor of 1/3 indicates the two-dimensional nature of current flow from the accumulation layer into the bulk N^- region [2.23,2.24] and models the conversion of current flow from lateral to vertical. More accurately, as illustrated in Fig. 2.2, the depletion-mode device should be modeled as a distributed structure. The derivation of this factor is considered in Fig. 2.11 where the current flows horizontally into the resistive element and out vertically along the element.

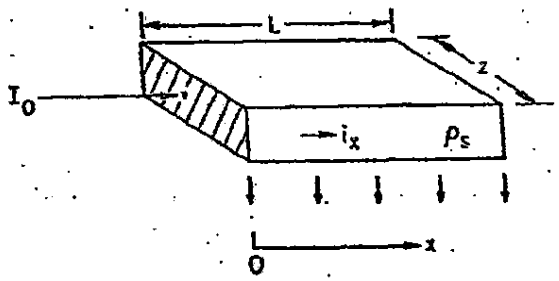


Fig. 2.11. MODEL USED IN THE CALCULATION OF DEPLETION-MODE ON-RESISTANCE.

The power loss caused by a transverse current i_x is

$$dP = \frac{i_x^2 \rho_s dx}{Z} \tag{2.14}$$

where ρ_s is sheet resistivity and Z is the width of the element. Assuming that the current flows uniformly along the element,

$$i_x = \frac{I_o(L - x)}{L} \tag{2.15}$$

where L is the length of the element. Substituting Eq. (2.15) into (2.14) after integrating the total power loss, P becomes

$$P = \int_0^L dp = \frac{I_o^2 \rho_s}{Z}\left(\frac{L}{3}\right) \tag{2.16}$$

which indicates that the equivalent length of the resistance is L/3.

For the photomicrograph in Fig. 2.4b, W = 3440 μ as before, L_T (defined in Fig. 2.10) is ≈20 μ, C_o is determined from the gate-oxide thickness of 950 Å, and V_{TD} depends on the epitaxial-layer doping concentration. The factor of 2 in the L'_{eff} definition in Fig. 2.10a does not appear in Eq. (2.13) because two devices effectively act in parallel.

Majority-carrier electron mobility in the surface accumulation layer is a parameter not as well characterized in the literature as inversion-layer mobility. Based on the work of Reddi [2.25] and more recently obtained additional data [2.5], a value of μ_D = 1050 cm^2/Vsec for the <100> surface at V_G = 0 was chosen. Note that this is not the limiting value of μ_D for $V_G - V_{TD} = 0$ because V_{TD} is approximately -2 V. A formulation similar to that for μ_E [2.19,2.5] was used to account for the reduction in μ_D as the gate field is increased.

Derivation of the JFET component of the VDMOS equivalent circuit (Fig. 2.2) is based on the geometry in Fig. 2.10a. The PN junction is modeled as a portion of a circle with the origin offset from the original mask edge by 0.15 X_j (junction depth of channel diffusion) to account for the difference in lateral and vertical diffusions. The current is assumed to originate uniformly from the surface accumulation layer. If X is positive downward from the surface, the spacing between the two P' diffusions becomes

$$L(X) = L - 2\sqrt{r_o^2 - x^2} \qquad (2.17)$$

where $L = L_T + 0.3\,X_j$ and r_o is the radius of the circle in Fig. 2.10a. Taking depletion regions that may exist in the n^- region into account, $r_o = X_j + X_d$. The width of the depletion layer is

$$X_d = \left[\frac{2\epsilon_{si}}{qN_D}(V_{DS} + \phi_B)\right]^{1/2} \qquad (2.18)$$

where V_{DS} is the drain-source voltage and ϕ_B is the built-in potential of the channel-drain p^+-n^- junction.

Current density as a function of X is

$$J(X) = \frac{I}{WL(x)/2} = \frac{1}{\rho}\frac{dv}{dx} \qquad (2.19)$$

By substituting Eq. (2.17) into (2.19) and integrating, the total resistance of the JFET region becomes

$$R_{JFET} = \int_0^V \frac{dv}{I} = \frac{\rho}{W/2}\int_0^{X_A} \frac{dx}{L - 2\sqrt{r_o^2 - x^2}} \qquad (2.20)$$

where X_A is equivalent to $\theta = 45°$. After conversion to the following polar coordinates,

$$x = r_o \sin\theta$$

$$dx = r_o \cos\theta\, d\theta$$

$$\sqrt{r_o^2 - x^2} = r_o \cos\theta$$

$$x = 0 \qquad \theta = 0$$

$$x = X_A \qquad \theta = \pi/4$$

Eq. (2.20) can be rewritten as

$$R_{JFET} = \frac{\rho}{W/2}\frac{r_o}{L}\int_0^{\pi/4}\frac{\cos\theta d\theta}{1 - 2/L\, r_o \cos\theta} \qquad (2.21)$$

Straightforward integration yields

$$R_{JFET} = \frac{2\rho}{W}\left[\frac{1}{\sqrt{1 - (2r_o/L)^2}}\tan^{-1}(0.414)\sqrt{\frac{L + 2r_o}{L - 2r_o}} - \frac{\pi}{8}\right] \qquad (2.22)$$

which applies for low V_{DS} (see Section H for high V_{DS}).

The JFET region of the VDMOS is considered to end at the point where $\theta = 45°$. Below this boundary in the N^- material, a bulk resistor bounded by the trapezoidal geometry in Fig. 2.10a represents the series resistance of the epitaxial layer.

For long stripes of interdigitated structure, the procedure for calculating this trapezoidal volume resistance is similar to the one followed for the JFET region. Current density as a function of vertical distance x is

$$J(x) = \frac{I}{W/2\ (a + 2\tan\alpha x)} \qquad (2.23)$$

where

I = current in the trapezoid

a = upper width of the trapezoid

α = spreading angle

The electric field is

$$E(x) = \rho J(x) \qquad (2.24)$$

and R_4 then becomes

$$R_4 = \frac{1}{I}\int_0^h E(x)\, dx \qquad (2.25)$$

Substituting Eqs. (2.23) and (2.24) into (2.25) yields

$$R_4 = \frac{\rho}{W} \frac{1}{\tan \alpha} \ln \left(1 + 2 \frac{h}{a} \tan \alpha\right) \qquad (2.26)$$

where h is the height of the trapezoid. The spreading angle is analogous to the thermal-impedance spreading angle derived by David [2.26]. His exact calculations can be approximated within ±5 percent by

$$\alpha = \begin{cases} 6.131^\circ \ln \left(200.444 \frac{h}{a}\right) & \frac{h}{a} \leq 4.0 \\ 41^\circ & \frac{h}{a} > 4.0 \end{cases} \qquad (2.27)$$

which was used in the modeling here.

For short stripes of trapezoids common in commercial layouts, the edge effect of two trapezoidal ends should be considered. The cross-sectional area of $A(x)$ in Fig. 2.12 is

$$A(x) = (a + 2 \tan \alpha \cdot x)(b_1 + 2 \tan \alpha \cdot x) \qquad (2.28)$$

where b_1 is the length of the trapezoid. Following a similar procedure used to calculate the long-stripe structure, R_4 becomes

$$R_4 = \int_0^h \frac{\rho \, dx}{(a + 2 \tan \alpha \cdot x)(b_1 + 2 \tan \alpha \cdot x)} \qquad (2.29)$$

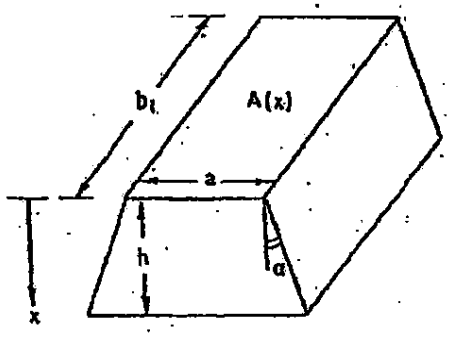


Fig. 2.12. CROSS SECTION OF EPITAXIAL DRIFT REGION.

Straightforward integration yields

$$R_4 = \begin{cases} \dfrac{\rho}{(b_1 - a)\ 2 \tan \alpha} \left[\ln\left(\dfrac{b_1}{a}\right) - \ln\left(\dfrac{b_1 + 2h \tan \alpha}{a + 2h \tan \alpha}\right) \right] & b_1 > a \\ \dfrac{\rho}{a \cdot 2 \tan \alpha} \left(1 - \dfrac{1}{1 + h/a \cdot 2 \tan \alpha}\right) & b_1 = a \end{cases} \qquad (2.30)$$

For $b_1 >> a$, Eq. (2.26) can be used with little error; for example, if $b/a = 10$ and $h = a$, only a 5 percent error would result. For $b_1 = a$ (square-top trapezoid), the error will be substantial when h/a is greater than 0.6. Figure 2.13 plots the ratio of R_4 [Eq. 2.30)]/R_4 [Eq. (2.26)] as a function of h/a.

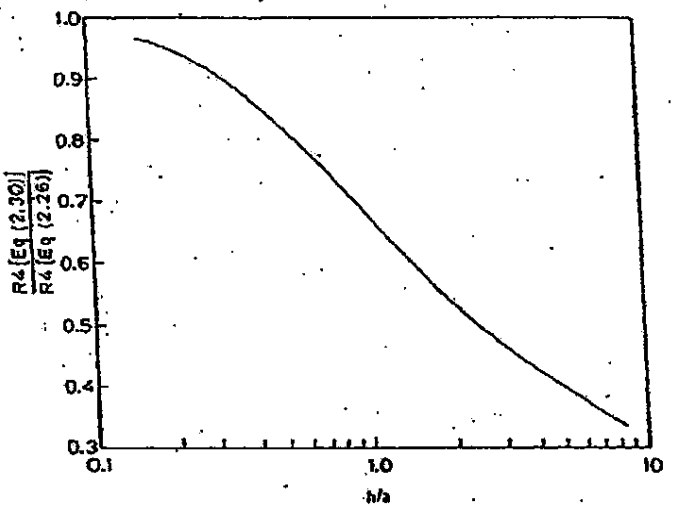


Fig. 2.13. RATIO OF EPITAXIAL BULK RESISTANCE CALCULATED IN EQ. (2.30) TO THAT IN EQ. (2.26) VS h/a.

If the epitaxial layer is very thick or if the surface packing density is high, adjacent trapezoids may overlap as in Fig. 2.16c. The resistance of region ⑤ can be determined by assuming uniform current flow in the merged region.

The model for on-resistance described above was applied to the VDMOS in Fig. 2.4b, and the results are plotted in Fig. 2.14; epitaxial thicknesses and L_{eff} values are the same as in Table 2.1. Channel width was always 3440 μ. Over a wide range of epitaxial resistivities, agreement with the experimental measurements was excellent. As with the LDMOS, the discrepancy between experiment and theory was most pronounced at small $V_G - V_{TE}$—most likely the result of the ineffectiveness of the surface accumulation layer to prevent current crowding at the end of the channel at low values.

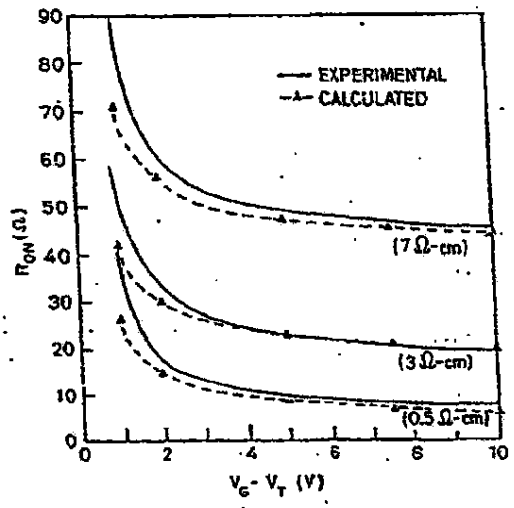


Fig. 2.14. ON-RESISTANCE OF THE VDMOS VS $V_G - V_{TE}$.

It is possible to evaluate the contributions of the various parts of the VDMOS equivalent circuit to overall on-resistance, and Fig. 2.15 is an example. For this calculation, the P-channel and N^+ junction depths were assumed to be 4 and 2 μ, respectively. This gives an L_{eff} of ≈1.7 μ, and L_T was assumed to be 20 μ. For each resistivity, an appropriate epitaxial thickness was determined from Fig. 2.5. Figure 2.15 plots the percentage of total on-resistance resulting from the

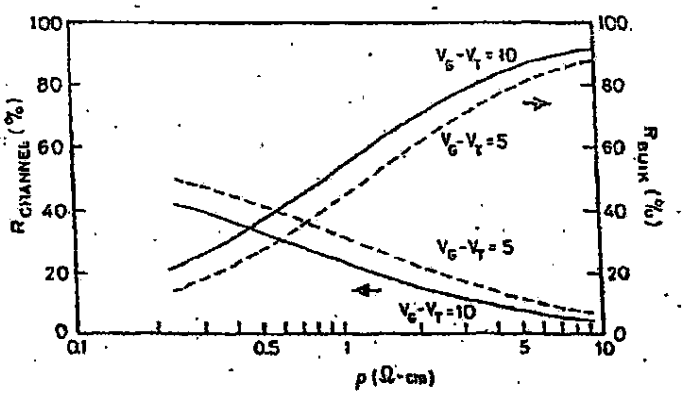


Fig. 2.15. CALCULATED PERCENTAGE OF TOTAL VDMOS ON-RESISTANCE.

enhancement channel R_E and from the sum of the JFET and bulk-resistance terms ($R_{JFET} + R_4$). The contribution of the depletion-mode device is simply the difference between 100 percent and the sum of the other two terms.

The results obtained from these calculations were not unexpected. In low-voltage devices ($\rho < 1$ Ω-cm), channel resistance is predominant and, in high-voltage structures, the bulk contributions of the JFET and the epitaxial layer dominate; in practice, when epitaxial resistivities are greater than 8 to 10 Ω-cm, overall on-resistance can be reasonably calculated from the bulk terms only.

The mask spacing between the P-type diffusion L_T is critical in determining the on-resistance of the JFET and the bulk epitaxial-resistor portions of the VDMOS equivalent circuit. In high-voltage structures (8.5 Ω-cm) where these two components dominate, L_T is a significant parameter in optimizing device performance, as can be seen in the experimental results in Fig. 2.16. These measurements were obtained from smaller-geometry devices (W = 200 p) which accounts for the higher values of on-resistance. In low-voltage devices (0.5 and 1.1 Ω-cm) where channel rather than bulk resistance dominates; however, L_T is not as critical. It is not desirable to arbitrarily increase L_T in high-voltage devices, however, because this will reduce total channel width (and, therefore, increase on-resistance). For a given epitaxial resistivity

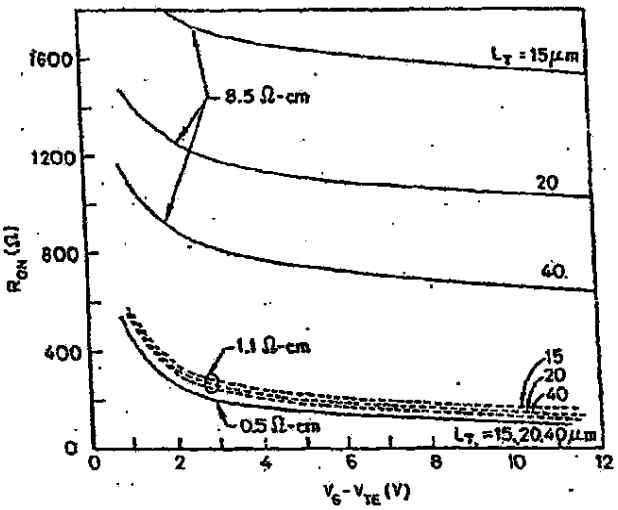


Fig. 2.16. EFFECT OF P-CHANNEL DIFFUSION SEPARATION L_T ON VDMOS ON-RESISTANCE.

and chip area, an optimal value for L_T should be established, which will minimize on-resistance. This will be demonstrated in Section F.

3. VMOS

Calculation of on-resistance in the VMOS is illustrated in Fig. 2.17. The thin gate oxide normally extends down to the bottom of the groove, which results in a surface accumulation layer under the gate where the groove extends into the N^- region. As in the VDMOS, this property tends to minimize current crowding at the end of the enhancement channel and, therefore, reduces on-resistance. This region should be modeled as a distributed network of depletion-mode transistors in series with bulk resistors; however, for simplicity, the same single-transistor/series-resistor model used in the VDMOS was employed here.

The overall on-resistance of the VMOS, therefore, is

$$R_{ON_{VMOS}} = R_E + R_D + R_3 + R_4 \qquad (2.31)$$

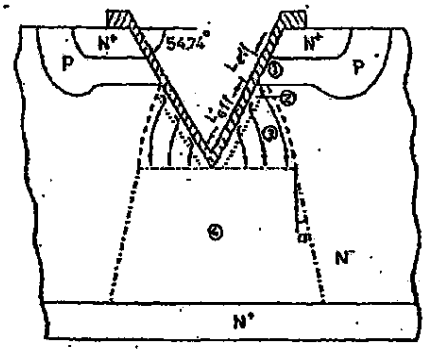


Fig. 2.17. MODEL OF THE VMOS USED TO CALCULATE ON-RESISTANCE. The device is separated into four series components.

where

R_E = enhancement-mode on-resistance, as defined in Eq. (2.10)

R_D = depletion-mode on-resistance (surface accumulation layer), as defined in Eq. (2.13)

R_3 = bulk resistance of region ③

R_4 = bulk resistance of trapezoidal region ④

The parameters are similar to those for the LDMOS and VDMOS except for L_{eff} and μ. The channel length in the VMOS is ≈1.5 times longer than those in the LDMOS and VDMOS. Both the inversion-layer mobility μ_E and the majority-carrier accumulation-layer mobility are smaller on the <111> surface of the VMOS than they are on the <100> surfaces of the other two; 80 percent of the corresponding numbers on the <100> plane were used for the VMOS [2.5,2.6] with the same reduction factors to account for the gate electric field in the LDMOS and VDMOS.

The bulk resistance of region ③ in Fig. 2.17 can be calculated by assuming that the geometry is a sector of a circle with an included angle of 54.7°. The current is also assumed to enter this region uniformly from the surface accumulation layer under the gate. Using the apex of the VMOS as the origin of the cylindrical coordinate, the voltage in region ③ is

$$V(r) = \int_0^{54.7°} rE \, d\theta \qquad (2.32)$$

where r is the radial distance from the origin and

$$E = \frac{Ip}{L'_{eff}(W/2)} \qquad (2.33)$$

is the electric field. The bulk resistance in region ③ R'_3 can now be calculated as

$$R'_3 = 2R_3 = \frac{V}{I} = \frac{1}{I}\frac{1}{L'_{eff}} \int_0^{L'_{eff}} V(r)\, dr \qquad (2.34)$$

The factor of 2 in front of R_3 indicates that two resistors R'_3 act in parallel in the VMOS equivalent circuit. Substituting $V(r)$ from Eq. (2.32) into (2.34) and straightforward integration yields

$$R_3 = 0.477 \frac{\rho}{W} \qquad (2.35)$$

Region ④ in the VMOS is identical to R_4 in the VDMOS device, and its resistance was derived in Eq. (2.26). The same considerations regarding the overlap of adjacent trapezoids described in Fig. 2.10c apply here.

The theoretical and experimental on-resistances of this VMOS at various epitaxial resistivities are compared in Fig. 2.18. The width of the mask opening for the V-groove etch was 10 μ. The agreement at high gate voltages is excellent. As $V_G - V_{TE}$ approaches zero, however, the divergence between theory and experiment becomes apparent, as was also observed in the LDMOS and VDMOS. Again, this behavior is believed to be the result of the failure of these models to account for current crowding at the end of the enhancement channel, particularly at low V_G where the surface accumulation layer is not as effective in reducing this crowding.

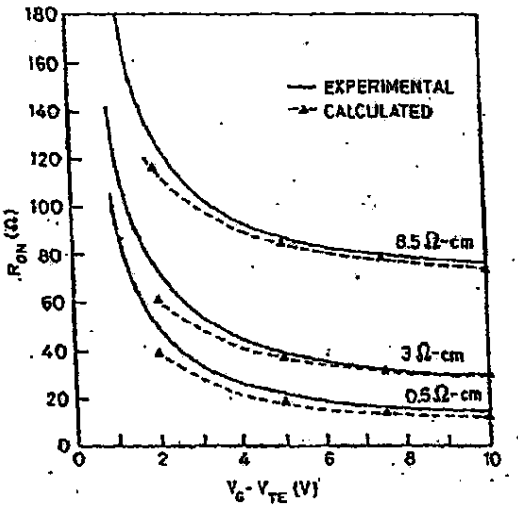


Fig. 2.18. ON-RESISTANCE OF THE VMOS VS $V_G - V_{TE}$.

The effect of V-groove depth for a given P-channel junction depth on on-resistance is plotted in Fig. 2.19; these calculations are for the 8.5 Ω-cm, 26.8-μ epitaxial-layer device in Fig. 2.18. The overall on-resistance (vertical scale) is normalized to the value achieved for a nominal 10 μ mask dimension. As L drops below 10 μ, on-resistance increases because of severe current crowding at the end of the enhancement channel, and the surface accumulation layer becomes less effective as its length is reduced. For L < 7 μ, the V-groove does not completely penetrate the channel diffusion and the on-resistance becomes infinite. This dependence of R_{ON} on L should be less pronounced in low-voltage devices where R_E tends to dominate; it should also be less pronounced at lower gate voltages for the same reason.

4. TVMOS

Another form of the VMOS is the truncated VMOS (TVMOS) structure [2.27]. As the SEM in Fig. 2.20 indicates, this device is fabricated by terminating the V-groove etch prior to reaching the apex of the groove, which requires a larger mask dimension, lower packing density, and better

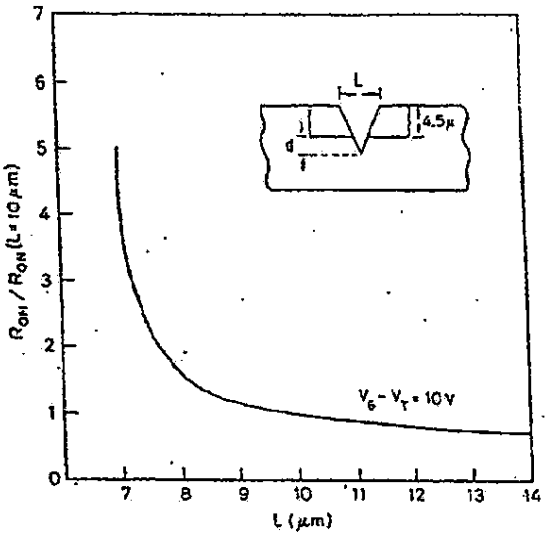


Fig. 2.19. CALCULATED EFFECT OF V-GROOVE DEPTH ON VMOS ON-RESISTANCE.

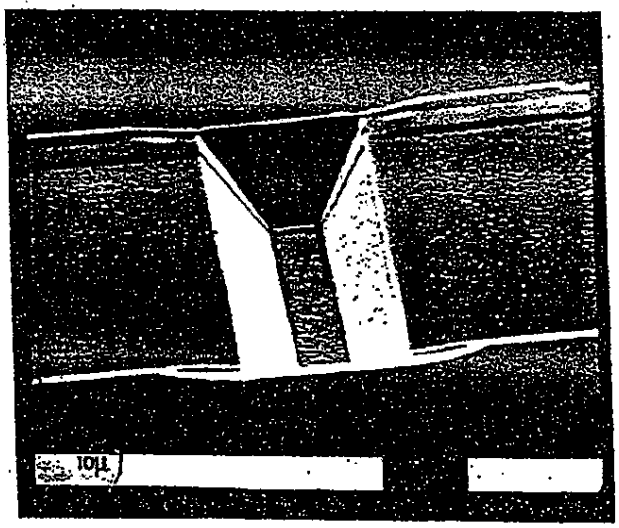


Fig. 2.20. SEM OF THE TRUNCATED V-GROOVE TVMOS.

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processing control than for the standard VMOS. The advantage here is that the flat-bottom portion of the V-groove behaves much like the surface accumulation region in the VDMOS by spreading out the current distribution and thereby reducing both current crowding and on-resistance.

The calculation of on-resistance in the TVMOS is illustrated in Fig. 2.21. The depth of the flat bottom can be seen to be beyond the depth of the P channel. Neglecting the small sections of circles used in VMOS modeling [R_3 in Eq. (2.35)], the TVMOS on-resistance is

$$R_{ON_{TVMOS}} = R_E + R_D + R_4 \qquad (2.36)$$

where

R_E = enhancement-mode on-resistance

R_D = depletion-mode on-resistance (surface accumulation layer)

R_4 = bulk resistance of trapezoidal region ④

The parameters L_{eff}, L'_{eff}, μ_E, and μ_D must be modified because of the differences in device geometry and crystal orientations; L'_{eff} is one-half of the lateral distance between the P channels, and μ_D is the accumulation-layer mobility on the <100> surface. Region ④ (R_4) is identical to those of the VMOS and VDMOS, and its on-resistance was derived in Eq. (2.26).

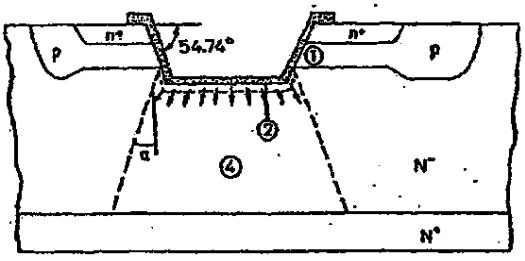

Fig. 2.21. MODEL OF THE TVMOS USED TO CALCULATE ON-RESISTANCE. The device is separated into three series components.

The advantage of the TVMOS can be seen in the experimental data in Fig. 2.22 where devices with 10 and 20 μ mask openings for the V-groove etch are compared in terms of on-resistance. Etching was terminated shortly after the 10 μ opening reached the bottom of its groove, which resulted in the 20 μ opening being etched approximately 7 to 8 μ deep with a flat-bottom length of ≈8 to 10 μ. The channel width was always 200 μ. In lower voltage devices (1.1 Ω-cm), this truncated structure offers little advantage because R_E dominates; in higher voltage devices (8.5 Ω-cm), however, the truncated geometry makes a significant difference because bulk resistances dominate. The spreading out of the current distribution by the accumulation layer at the groove bottom should be helpful here.

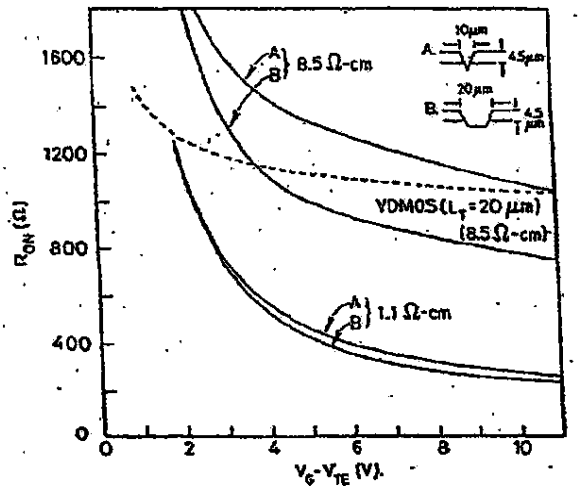

Fig. 2.22. COMPARISON OF THE ON-RESISTANCE OF VMOS DEVICES WITH BOTH FULLY ETCHED AND TRUNCATED V-GROOVES VS $V_G - V_{TE}$

For comparison, the on-resistance of a VDMOS fabricated in 8.5 Ω-cm epitaxy with W = 200 μ and L_T = 20 μ is also plotted in Fig. 2.22. Its shorter channel and higher electron mobility have the advantage in on-resistance at low gate voltages. At higher voltages where

bulk resistances dominate, the truncated VMOS is superior because the current in the VDMOS flows through the bulk material all the way from the surface down to the N^+ substrate; in the truncated VMOS, this distance is reduced by the nonplanar configuration.

5. Device Comparisons

The models discussed in this section facilitate the calculation of on-resistance in a number of planar and nonplanar power MOSFETs. Their comparative advantages are difficult to describe because these structures are highly dependent on technology and design rules (layout). The following observations, however, are based on the above modeling.

- In high-voltage applications, bulk resistance completely dominates overall on-resistance. This tends to mask any device differences resulting from mobility and scattering-limited velocity variations with crystal orientations and doping levels. At very high voltages, the selection of a specific structure will be based on layout efficiency and technology rather than on such parameters as μ_E and v_{SAT}.
- In low- and moderate-voltage applications, the LDMOS and VDMOS are superior in terms of electron mobility in the active channel which implies that, for a given channel width, these devices will exhibit lower on-resistance when R_E and R_D dominate. This advantage may be obviated, however, by layout considerations because the overall goal is to achieve a specified on-resistance in a minimum chip area.

F. Application of On-Resistance Models to Power-MOSFET Design

The on-resistance models of the LDMOS, VDMOS, and VMOS have the potential of becoming very powerful tools in power-MOSFET design. It is apparent that the primary objective is to minimize on-resistance; however, the following variations in emphasis are dependent on the breakdown-voltage requirement.

- For high-voltage devices, the goal is to minimize bulk resistance.
- For low-voltage devices, the goal is to maximize the W/L_{eff} ratio for a given chip area.

One example of an application of these models is a commercial power FET known as the HEXFET [2.28]. Its structure is a vertical DMOS (VDMOS) consisting of many nested cells of hexagonal geometry as illustrated in Fig. 2.23.

For simplicity, a rectangular vertical geometry (Fig. 2.24) was chosen to account for the portion of JFET resistance. This modification helps to simplify the mathematical calculation of R_{ON} which, when calculated, will be slightly higher than the measured value because of the lack of curvatures in the diffused junctions.

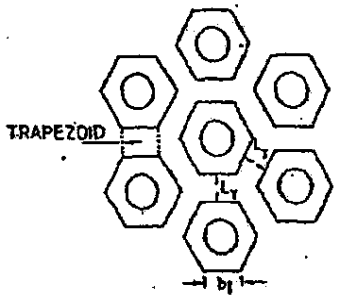

Fig. 2.23. HEXFET TOPOLOGY. Here, b_1 is the length of one side of a hexagon and L_T is the spacing between the p-wells.

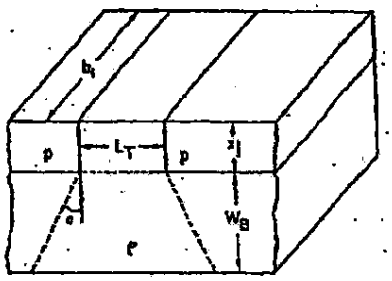

Fig. 2.24. SIMPLIFIED CROSS SECTION OF THE HEXFET.

The cell area of the hexagon in Fig. 2.23 is

$$A_{cell} = \frac{3\sqrt{3}}{2}\left(b_1 + \frac{L_T}{\sqrt{3}}\right)^2 \qquad (2.37)$$

where b_1 is the cell width, L_T is gate width, and the cell boundary is halfway between the adjacent cells. The total number of cells for a given chip area A is

$$N_{cell} = \frac{A}{A_{cell}} \qquad (2.38)$$

Two adjacent hexagons form a "trapezoid" as described in Fig. 2.23, and the number of these trapezoids for a given chip area then becomes

$$N_T = 3N_{cell} \tag{2.39}$$

The areas between adjacent trapezoids are not considered in these calculations. The reason for calculating N_T is that, in high-voltage applications (breakdown voltages greater than 300 V), overall on-resistance is dominated by bulk resistance, and only R_{JFET} and R_{EPI} must be considered. In low-voltage applications, the MOS channel contribution must also be taken into account. After this is determined, total on-resistance becomes

$$R_T = \frac{(R_{JFET} + R_{EPI}) \text{ of one trapezoid}}{N_T} \tag{2.40}$$

where $R_{JFET} = \rho X_j / b_1 L_0$ and

ρ = resistivity of epitaxial layer

X_j = p-well depth

$L_0 = L_T - 2(X_d + 0.85\, X_j)$

R_{EPI} = epitaxial bulk resistance [Eq. (2.36)]

After substituting Eqs. (2.37), (2.38), and (2.39) into (2.40),

$$R_T = \frac{\sqrt{3}}{2A}\left(b_1 + \frac{L_T}{\sqrt{3}}\right)^2 (R_{JFET} + R_{EPI}) \tag{2.41}$$

Normalized by $\sqrt{3}/2A$, R_T then becomes

$$\hat{R}_T = \left(b_1 + \frac{L_T}{\sqrt{3}}\right)^2 (R_{JFET} + R_{EPI}) \tag{2.42}$$

After the breakdown voltage has been established, epitaxial thickness W_B and resistivity can be determined from Eq. (2.3). The problem

then becomes one of optimizing the two independent variables b_1 and L_T to obtain a minimum value for $\hat{R}_T$ over a certain range of b_1 and L_T. One of the industrial standard 450 V (breakdown voltage) devices is used to illustrate the application procedures. To achieve the final 450 V requirement, the 550 V ideal parallel-plane breakdown voltage will accommodate the approximately 15 percent loss in voltages caused by the edge effects and processing variations. Under this condition, the effective epitaxial thickness (between the p-well and N^+ substrate) becomes 33.57 μ and epitaxial resistivity is 13.67 Ω-cm.

To determine the minima of the function $f(x,y)$ [2.29] requires simultaneous solutions of

$$\frac{\partial f}{\partial x} = 0 \qquad (2.43)$$

and

$$\frac{\partial f}{\partial y} = 0 \qquad (2.44)$$

which should satisfy the following criteria:

$$\left(\frac{\partial^2 f}{\partial x \partial y}\right)^2 - \frac{\partial^2 f}{\partial x^2}\frac{\partial^2 f}{\partial y^2} < 0$$

and

$$\frac{\partial^2 f}{\partial x^2} > 0$$

Based on this condition and with $X_j = 3$ μ and $X_d = 1.58$ μ for $1\ \mu \leq b_1 \leq 30\ \mu$ and $10\ \mu \leq L_T \leq 40\ \mu$, the minimum value of $\hat{R}_T$ was found to be 4.37×10^{-2} Ω-cm^2 at $b_1 = 6$ μ and $L_T = 18$ μ. If chip area A is 0.0746 cm^{-2}, for example, $R_{T(min)}$ will be 0.51 Ω. The value achieved in the commercial 400 V HEXFET (IRF330) is 0.9 Ω. This discrepancy is probably the result of the differences in X_j, b_1, and L_T and the omission of channel resistance in the calculations.

In Fig. 2.25, $\hat{R}_T$ is plotted as a function of L_T for various values of b_1. As L_T is reduced, the number of cells increases; however, current crowding will raise the on-resistance enormously. On the other

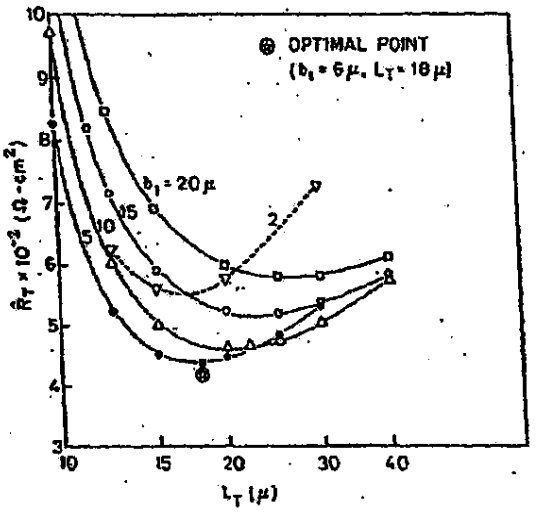

Fig. 2.25. NORMALIZED ON-RESISTANCE VS GATE WIDTH FOR VARIOUS CELL WIDTHS.

hand, if L_T becomes too large, the number of cells will drop even though the individual JFET and epitaxial resistances are small, and this will also contribute to the on-resistance. As a result, there is an optimal point in L_T at which a minimum $\hat{R}_T$ can be established for a given b_1. It can be seen in Fig. 2.25 that on-resistance increases more rapidly if the gate dimension is too narrow rather than too wide.

In Fig. 2.26, $\hat{R}_T$ is plotted as a function of b_1 for various values of L_T. For the same reasons as in Fig. 2.25, there is an optimal point in b_1 at which a minimum $\hat{R}_T$ can be obtained for a given L_T.

It becomes apparent in Figs. 2.25 and 2.26 that there are optimal gate and cell widths for a given epitaxial-layer resistivity and channel junction depth. A specific geometry and resistivity have been selected in this section to illustrate the optimization of layout dimensions via the on-resistance model. These models are also applicable to other geometries.